A NEW PWM TECHNIQUE FOR REDUCING SINGLE PHASE CURRENT AND MAKING THREE PHASE CURRENT ZERO FOR MULTILEVEL INVERTER

S.DEVI LAVANYA[1] ,Dr.D. KIRUBAKARAN[2]

ABSTRACT - The paper is focused to reduce single phase current and make three phases current zero by using a suitable PWM technique for a three phase Multilevel inverter and making it suitable for electrical drives. The paper uses a new technology that is using the carriers of different amplitude and all the carriers of same frequency operating at higher frequencies and adding a summer in the PWM technique. The proposed PWM technique is simple and easy to understand and the number of components is reduced highly this is achieved by adding a summer as explained. The paper is concentrated not to use any filter the reason behind this is that it increases the single phase current to a very high value which is very dangerous this is avoided in proposed topology. The advantages and disadvantages of these PWM techniques are compared with other PWM techniques in this paper and it uses new NPC H-Bridge inverter.

Key words - PWM technique, multilevel inverters, reduced components, summer, single phase and three phase current, Ac power generation, HVDC, NPC H-Bridge inverter.

1. INTRODUCTION

Multilevel voltage source inverters are a new generation of power inverters suitable for high power and high voltage applications because of reduced harmonic contents and low voltage stress across load. In this paper, a novel predictive PWM control technique is proposed for a three-phase multilevel inverter, which Controls the capacitors' voltage and load current with low switching losses. This method also controls the capacitor voltage in order to minimize switching losses. The advantage of this contribution is that it reduces the number of components highly the reason is that it uses a summer in the PWM technique which reduces the number of components also reducing single phase current and making three phase current zero. The power electronics is a device which converts DC power to AC power at required outputvoltage and frequency level is known as an inverter. The inverters can be broadly classified as two level inverters and multilevel inverters.

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One advantage that multilevel inverters have compared to two level inverters is minimum harmonic distortion. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator; HVDC and machine drive for sinusoidal and trapezoidal current applications. This paper focuses on the analysis of PWM technique for Multilevel inverter by reducing the number of components highly this is achieved by adding summer to the PWM technique which reduces the number of components highly. A seven-level inverter had been simulated by Matlab/Simulink in different ways. The proposed topology does not use any clamping diodes which is an added advantage reducing the number of components and uses only one flying capacitor for each phase. The PWM technique employed in this topology is simple and easy to understand when compared to SVPWM which makes the circuit analysis complicated. The various switching strategies that have been proposed for synthesizing output voltage with minimum distortion, sinusoidal pulse width modulation (SPWM) strategy is employed. In this method, number of triangular waveforms is compared with a reference sinusoidal modulating signal and the switching rules for the switches are decided by the intersection of the carrier waves with the modulating signal. For a 7-level inverter, a modulating signal and 6 carrier waves are required for each phase of the inverter.

All of the carriers have the same frequency f_c and different amplitude *Ac*, while the modulating signal has a frequency of *fm* and amplitude of *Am*. F*c* should be of very

high value compared to *fm*. The amplitude of the modulated wave is greater than the amplitude of the carrier. A seven step bridge is used for three phase inverter by using 30 switches, 10 switches for each phase. Each step is defined as a change in the time operation for each transistor to the next transistor in proper sequence.

As per [1] it requires a more number of filters and more number of chargeable capacitor for capacitor voltage balancing. But the proposed topology reduces the number of filter and reduces the number of components highly which does not use more number of capacitors and use less number of chargeable capacitors. As the name suggests that this is a five level inverter but the output obtained is sinusoidal this is because of summer added in PWM technique. As per [2] it requires the clamping diodes to clamp the voltage to a particular value but the proposed topology does not use any diodes to clamp the voltage. The control signals used here are easy for analysis which requires the analysis of less number of switching states. Figure. (C). Shows the output of other PWM techniques we can observe in figure (C) there is a level shift when we use previous PWM techniques when it is approaching a sinusoidal waveform. But in the proposed PWM technique such thing does not take place a pure sinusoidal waveform without level shift can be obtained. There is level shift occurring because of level shift carrier but the proposed topology has a carrier of the form shown in figure.6. and also output shows that triangular carrier has better performance compared to ramp wave as a carrier.

II. DESIGN OF THE PROPOSED TOPOLOGY

The input dc voltage given to the proposed topology is equal to V_{dc} which is clamped to $+V_{dc}/2$ and $-V_{dc}/2$ using capacitors, which is further clamped to $+V_{dc}/4$ and $-V_{dc}/4$ for the next stage given by means of chargeable capacitor the output of which is given to the three phase load. The value of the capacitor used is 10 farads acting as a dc source. As the number of levels increases the value of the capacitance decreases. The load used here is R and RL type of load. The

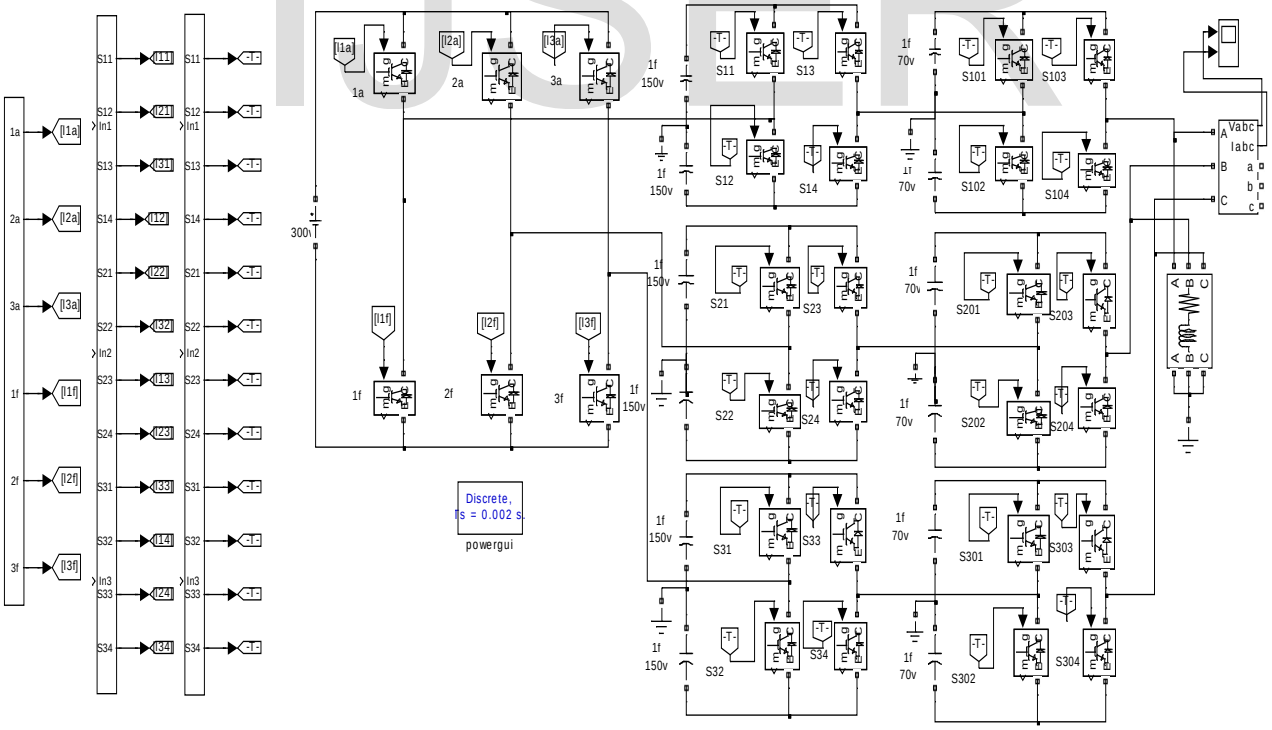

FIGURE 1. MATLAB/SIMULINK CIRCUIT FOR THREE PHASE MULTILEVEL INVERTER

Value of all the capacitors used is around 20 farads.

3. SIMULATION ANALYSIS

The power circuit diagram of a three phase full bridge inverter is shown in Fig (1). DC supply for three phase inverters is taken from a battery or usually from a rectifier. A circuit is obtained using 30 switches and 10 IGBTs in each phases. The proposed topology is analyzed using MATLAB/SIMULINK software using two types of load R and RL. The out voltage and current waveforms are as shown in Fig (5) and FFT window.

4. 4.PWM TECHNIQUE

The PWM technique employed in this topology is obtained using carrier based PWM technique which is shown in Fig (2a) and Fig (2b). In this technique the sine wave is used as a reference wave which is compared with a logical comparator operator and which output is compared with a repeating sequence TRIANGULAR wave using the logical not operator the output of this is given to the summer. The amplitude of the reference required is high compared to carrier.

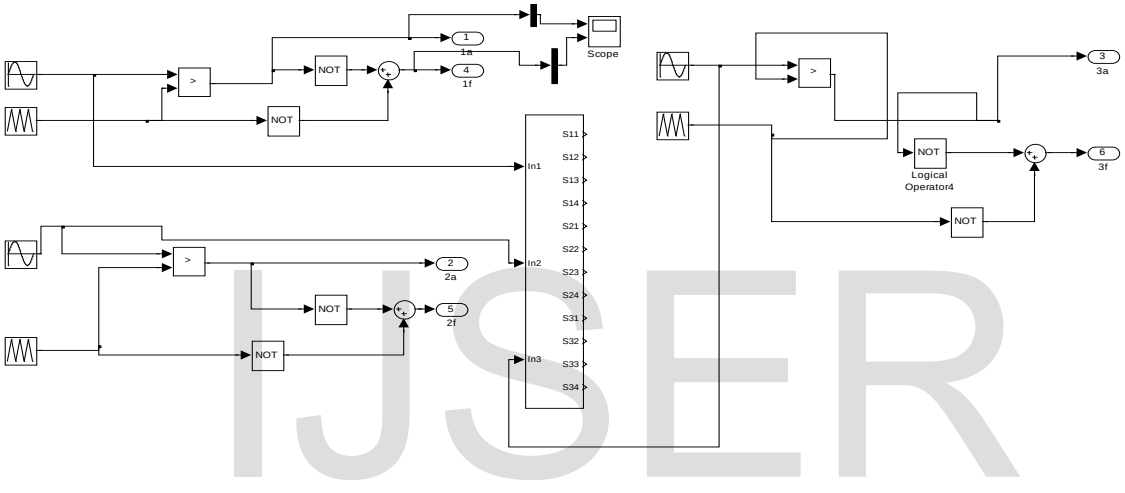

FIGURE 2a. PWM SIGNALS GIVEN TO A THREE PHASE TWO LEVEL INVERTER

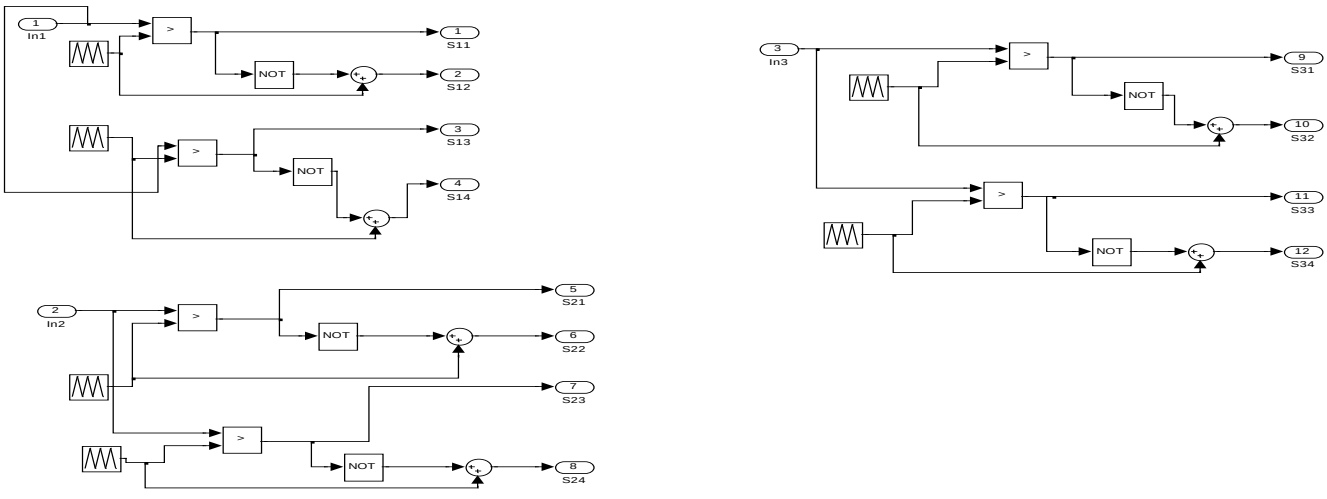

FIGURE 2b. PWM SIGNALS GIVEN TO H-BRIDGE INVERTER

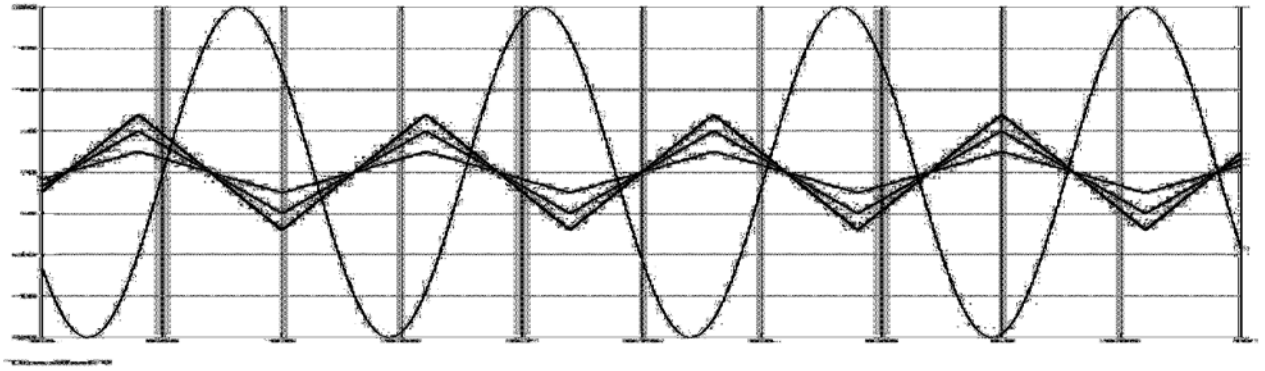

FIGURE.3. A NEW PWM TECHNIQUE

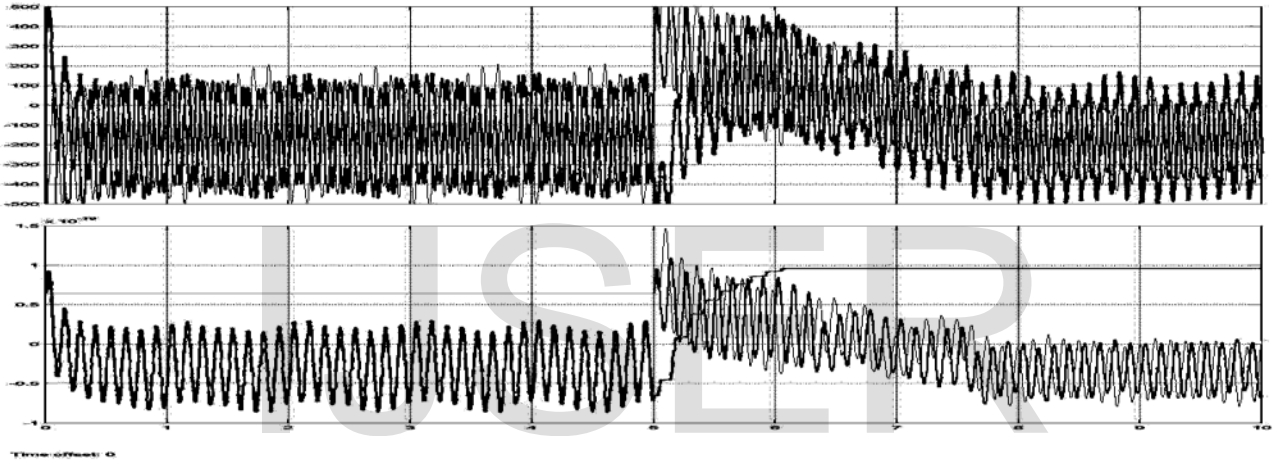

FIGURE.4. OUTPUT OF OTHER PWM TECHNIQUES

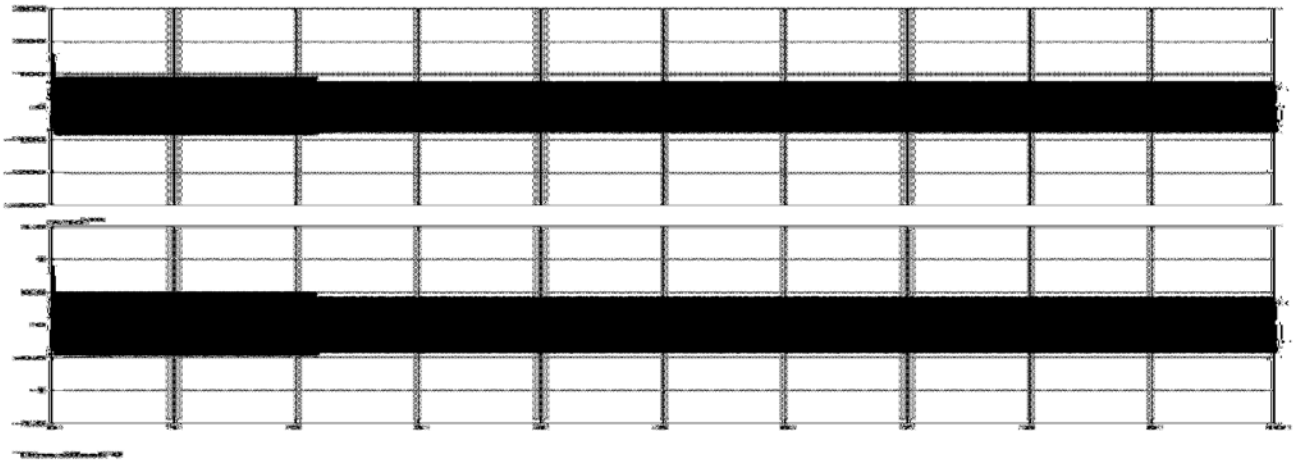

FIGURE.5. OUTPUT OF PROPOSED PWM TECHNIQUES

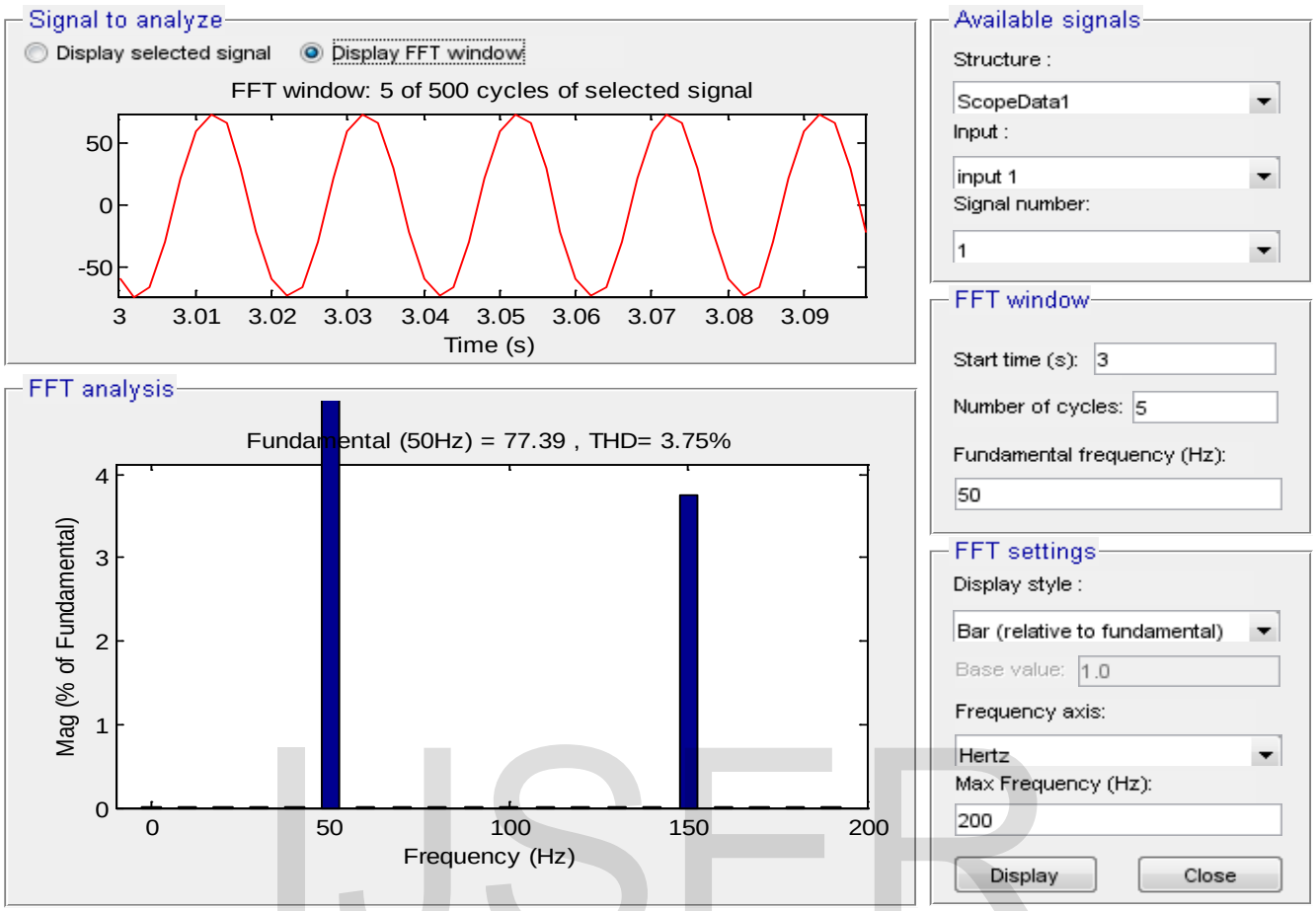

FIGURE.6. THD=3.75%

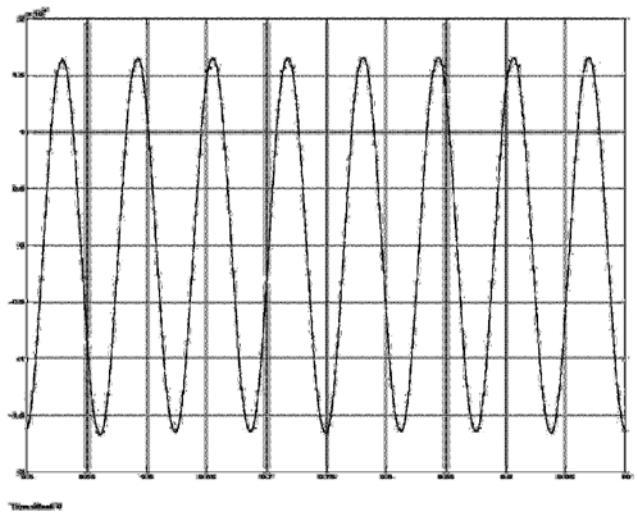

FIGURE.7. SINGLE PHASE CURRENT=2x10⁴

5. COMPARISION WITH OTHER TOPOLOGIES

Figure (4) and (5) shows the comparison with other topologies. Figure (5) is the output of the proposed PWM technique. Figure (7) shows that the single phase current is around $2x10^4$ amps when we use filter. Figure (C) shows that there is a level shift which does not take place in proposed topology. Figure (5) shows the three phase current is reduced to $5x10^{-4}$ and the single phase current is around 0.2amps and output voltage of around 30 volts for a dc voltage of 50volts. Figure (6) shows that the total harmonic distortion is around 3.75%.

6. CONCLUSION

The new PWM technique is invented in this paper which is obtained by adding summer which reduces the

number of components and single phase current highly and the three phases current is reduced totally the comparison with other PWM techniques is as shown. The output is obtained using a single dc source, so this topology can be used for ac power generation using solar panels as dc source and the proposed PWM technique can be implemented for further future extension and can be extended for a n number of multilevel inverter. Since the proposed topology converts DC to AC and the output obtained is sinusoidal verified using MATLAB/SIMULINK software it can be implemented for HVDC which is a promising issue of long distance transmission as the ac power cannot be stored also it cannot be transmitted over long distances as the THD=3.75% only it can be implemented for industries also the paper has used a new NPC H-bridge inverter as the number of H-bridge inverter is added the THD can be reduced also it can be made Zero and also the three phase current is totally zero.

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